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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/587,691	07/27/2006	Hannes P. Hofmann	EFFEP0101US	7045

7590 11/12/2009
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EXAMINER

NGUYEN, HUNG D

ART UNIT	PAPER NUMBER
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3742

MAIL DATE	DELIVERY MODE
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11/12/2009

PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No. 10/587,691	Applicant(s) HOFMANN, HANNES P.	
	Examiner HUNG NGUYEN	Art Unit 3742	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 31 July 2009.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-22 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-22 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 27 July 2006 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☒ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413) |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | Paper No(s)/Mail Date. _____ |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08) | 5) <input type="checkbox"/> Notice of Informal Patent Application |
| Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

2. Claims 1-15 and 18-22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tamm (US Pat. 5,666,722) (Previously cited) in view of Tsushima (US Pub. 2004/0086806).

3. Regarding claims 1 and 12, Tamm discloses a structure having laser ablated features and method of fabricating comprising the following step:

- a) Providing a printed circuit board 20 (Fig. 3a);
- b) Coating the circuit board on at least one side thereof with a dielectric 21 and 22 (Fig. 2a) (Col. 4, Lines 62-65) to form a dielectric layer;
- c) Structuring the dielectric layer for producing a trenches 24, 25 and 26 (Fig. 2b) and vias 23a (Fig. 2c) therein using laser ablation (Col. 4, Line 66 to Col. 5, Line 2);
- e) Depositing a metal layer (Fig. 2d) onto the trenches and vias being completely filled with metal for forming conductor structures therein (Col. 5, Lines 11-14);
- f) Removing the metal layer and the primer layer (Fig. 2f) (Col. 5, Line 17-21),

except for in the trenches and vias, to expose the dielectric layer if the primer layer has been deposited onto the entire surface in method step d).

Tamm fails to show the trenches not extending completely through the dielectric layer and depositing a primer layer into the produced trenches and vias only.

Regarding claim 12, Tamm fails to show the primer layer is deposited by sputtering method.

Tsushima teaches the structuring the dielectric for producing a trenches 2b (Fig. 1c) using laser ablation (Par. 27), the trenches not extending completely through the dielectric (See Fig. 1d, the trench did not extending through layer 2); and depositing a primer layer into the produced trenches (Par. 31); and the primer layer is deposited by sputtering method (Par. 31).

It would have been obvious to one of ordinary skill in the art at the time of the invention was made to utilize in Tamm to have the trenches not extending completely through the dielectric layer and depositing a primer layer into the produced trenches and vias only; and the primer layer is deposited by sputtering method, as taught by Tsushima, for the purpose of improving adhesion of the metal film and the dielectric layer.

4. Regarding claim 2, Tamm further discloses a method of manufacturing printed circuit board where the trenches 24, 25, and 26 (Fig. 2b) and vias 23a (Fig. 2c) are produced in one single process operation (Col. 4, Lines 50-54; Col. 4, Line 66 to Col. 5, Line 2).

5. Regarding claim 3 and 20, Tamm further discloses a method of manufacturing printed circuit board where the trenches and vias are performed by a laser ablation with direct-writing technique (Col. 6, Lines 17-24).
6. Regarding claim 4, Tamm further discloses a method of manufacturing printed circuit board where the direct-write technique comprises scanning a laser beam across the dielectric layer at those surface regions of the dielectric in which the trenches and vias are to be produced (Col. 6, Lines 17-45).
7. Regarding claims 5 and 18, Tamm further discloses a method of manufacturing printed circuit board which adjusting the power of the laser beam to depend on the depth of the trenches and vias to be produced (Col. 3, Lines 38-40; Col. 6, Lines 45-47).
8. Regarding claim 6, Tamm further discloses a method of manufacturing printed circuit board where the direct-write technique further comprises pulsing the laser beam (Col. 3, Lines 29-33).
9. Regarding claim 7, Tamm further discloses a method of manufacturing printed circuit board where adjusting the energy amount of the laser beam irradiated to a surface area of the dielectric layer to depend on the depth of the trenches and vias to be produced by setting the number of laser pulses being irradiated to said surface area (Col. 3, Line 38-43).
10. Regarding claims 8 and 22, Tamm further discloses a method of manufacturing printed circuit board where the direct-write technique further comprises decreasing the energy amount of successive energy pulses being irradiated to a surface area of the dielectric layer (Col. 3, Line 38-43).

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11. Regarding claim 9, Tamm further discloses a method of manufacturing printed circuit board where the trenches are connected to another trenches in different layers for multilayer board (Fig. 2f).

12. Regarding claim 10, Tamm further discloses a method wherein further method steps are performed once or several times after method step f): g) Depositing another dielectric layer onto the dielectric layer being provided with trenches and vias; and h) Repeating the steps c through f (Fig. 1g; Col. 4, Lines 42-49).

13. Regarding claims 11 and 19, Tamm further discloses a method of manufacturing printed circuit board wherein a terminating layer 12 and 13 (Fig. 1g) is deposited after any one of method steps f or h (Col. 4, Lines 42-49).

14. Regarding claim 13, Tamm further discloses a method of manufacturing printed circuit board wherein the metal layer is formed by electroless plating (Col. 5, Lines 59-61).

15. Regarding claim 14, Tamm further discloses a method of manufacturing printed circuit board wherein the metal layer and the primer layer are removed by polishing (Col. 5, Lines 17-21).

16. Regarding claim 15, Tamm further discloses a method of manufacturing printed circuit board wherein producing trenches and vias in the dielectric in method step c comprises producing trenches, said trenches also comprising vias (Fig. 2b-2c).

17. Regarding claim 21, Tamm further discloses a method of manufacturing printed circuit board wherein a method of manufacturing printed circuit board where the printed

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circuit board is a multilayer circuit board comprising two sides and a conductor pattern on each side (Fig. 2f) (Col. 4, Lines 32-35).

18. Claim 16 is rejected under 35 U.S.C. 103(a) as being unpatentable over Tamm (US Pat. 5,666,722) in view of Tsushima (US Pub. 2004/0086806) and further view of Konrad et al. (US Pub. 2002/0129972) (Previously cited).

19. Regarding claim 16, the combined Tamm-Tsushima disclose substantially all features of the claimed invention as set forth above except for functional layers are deposited onto the metal layer for electrically contacting electric components. Konrad et al. discloses the functional layers are deposited onto the metal layer for electrically contacting electric components (Par. 49). It would have been obvious to one of ordinary skill in the art at the time of the invention was made to utilize in the combined references to have the functional layers are deposited onto the metal layer for electrically contacting electric components, as taught by Konrad et al., for the purpose of having a excellent conductive layer that makes contact with semiconductor chip.

20. Claim 17 is rejected under 35 U.S.C. 103(a) as being unpatentable over Tamm (US Pat. 5,666,722) in view of Tsushima (US Pub. 2004/0086806) and further view of Yokogawa et al. (US Pat. 6,740,416) (Previously cited).

21. Regarding claim 17, the combined Tamm-Tsushima disclose all the claimed features as set forth above except for the circuit carrier is manufactured in a horizontal line. Yokogawa et al. teaches aerogel substrate and method for preparing the same where the circuit carrier is manufactured in a horizontal line (Col. 18, Line 53 to Col. 19, Lines 8). It would have been obvious to one of ordinary skill in the art at the time of the

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invention was made to utilize in the combined references to have the circuit carrier is manufactured in a horizontal line, as taught by Yokogawa et al., for the purpose of simplifying the process of manufacture the printed circuit board.

Response to Arguments

22. Applicant's arguments with respect to claims 1-22 have been considered but are moot in view of the new ground(s) of rejection.

23. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire **THREE MONTHS** from the mailing date of this action. In the event a first reply is filed within **TWO MONTHS** of the mailing date of this final action and the advisory action is not mailed until after the end of the **THREE-MONTH** shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than **SIX MONTHS** from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to HUNG NGUYEN whose telephone number is (571)270-7828. The examiner can normally be reached on Monday-Friday, 9M-6PM EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tu Hoang can be reached on (571)272-4780. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/HUNG NGUYEN/
Examiner, Art Unit 3742
11/5/2009

/TU B HOANG/
Supervisory Patent Examiner, Art Unit 3742